What is Claimed:

1. A method of manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

applying a first test stress to selected cells of the plurality of memory cells with a built-in self test;

identifying at least one weak memory cell;

repairing the at least one weak memory cell; and

applying a second test stress to the selected cells and the repaired cells with the built-in self test.

2. The method of claim 1, wherein the step of applying a first test stress further comprises the step of operating the memory cells with a timing that exceeds an operational timing.

3. The method of claim 1, further comprising the step of applying the first test stress in at least one of a plurality of test sequences.

4. The method of claim 1, wherein the step of applying a second test stress includes the step of applying an operational timing.

5. The method of claim 1, further comprising the step of applying the second test stress in at least one of a second plurality of test sequences.

6. The method of claim 1, wherein the step of applying a first test stress includes the step of operating each memory cell with at least one tight timing, the at least one tight timing being shorter than an operational timing.

7. A method for testing during manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

applying a first set of timings to selected cells of the plurality of memory cells using built-in self test controls;

testing the selected cells using the first set of timings;

identifying weak memory cells;

repairing the weak memory cells;

applying a second set of timings to the selected cells and the repaired cells using the built-in self test controls; and

testing the selected cells and the repaired cells using the second set of timings.

8. The method of claim 7, wherein the first set of timings provides at least a first stress to the cells and the second set of timings provides at least a second stress to the cells.

9. The method of claim 8, wherein the second set of timings tests the memory cells at an operational timing.

10. The method of claim 8, wherein the first set of timings tests the memory cells at timings that are faster than an operational timing.

11. The method of claim 8, further comprising the steps of using the first set of timings to provide at least a third stress to the cells and using the second set of timings to provide at least a fourth stress to the cells.

12. A method of manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

(a) providing a first plurality of timings and a second plurality of timings to built-in self test controls;

(b) applying at least one of the first plurality of timings to selected cells using the built-in self test controls;

(c) identifying failed memory cells;

(d) repairing the failed memory cells; and

(e) repeating steps (b) to (d) by applying additional selected ones of the first plurality of timings to the cells.

13. The method of claim 12 further comprising the step of (f) applying at least one of the second plurality of timings to each of the cells using the built-in self test controls.

14. The method of claim 13 further comprising the step of (g) repeating step (f) by applying additional selected ones of the second plurality of timings to each of the cells.

15. A device for testing an embedded memory having a plurality of memory cells during manufacture of the embedded memory, the device comprising:

a first timer for applying a plurality of timings to the memory cells;

a second timer for modifying at least one of the plurality of timings; and

a logic circuit for testing the memory cells by applying the at least one of the plurality of timings to the memory cells.

16. The device of claim 15, further comprising a sensor coupled to the memory cells for determining whether the memory cells failed the testing; and a repair component for repairing failed cells.

17. The device of claim 15, wherein the first timer includes the second timer and the second timer includes a delay circuit for modifying the at least one of the plurality of timings.

18. The device of claim 17, wherein the first and second timers are located in at least one area of the embedded memory.

19. The device of claim 15, wherein the embedded memory includes a built-in self test for controlling the testing for determining whether any memory cells failed the testing.

20. The device of claim 19, wherein the embedded memory includes a built-in self repair for repairing failed memory cells.